Product/Process Change Notice - PCN 22_0234 Rev. -

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This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

PCN Title:	AD7124-4 Metal Edit and Assembly Site Change. Applies to TSSOP package only
Publication Date:	27-Feb-2023
Effectivity Date:	01-Jun-2023 *(the earliest date that a customer could expect to receive changed material)*
Revision Description:	Initial Release

Description Of Change:

Metal Edits to improve
1. Performance at -40'C with low power supply when there are large steps in the common mode voltage to the PGA.
2. Prevent a reset of the device when the analog input on a channel is outside the datasheet operating conditions and converting the internal 20mV diagnostic on another channel.

Other changes
1. ID Register value changed to 0x07
2. When V_20MV_P/ V_20MV_M is selected as the analog input to the ADC, the absolute voltage on V_20MV_M will be at AVSS which may cause the AINM_UV_ERR flag to be set (if AINM_UV_ERR_EN=1). So, if the AINM_UV_ERR check is enabled, the user should ignore the value of AINM_UV_ERR when the channel V_20MV_P/ V_20MV_M is being measured.
3. The re-designed silicon includes a pre-charge buffer which ensures that the first conversion after switching channels is settled. On the current silicon, there is no pre-charge buffer so at fast output data rates, the first conversion may not be completely settled if large resistive loads are placed on the analog input.
4. An additional excitation current of 100nA is included on the part. Setting the Excitation Current bits to b111 enables the 100nA current. This setting generated a 1mA excitation current on the previous silicon.
5. The excitation currents, if enabled, remain active in standby mode. The currents were automatically disabled in standby mode on the previous silicon.

Assembly Move:
1. Assembly location has changed from Amkor Philippines to ASE Chung Li.

Reason For Change:

Improve robustness and performance of the part and ensure continuity of supply.

Impact of the change (positive or negative) on fit, form, function & reliability:

No change to fit, form, function and reliability of the device.

Product Identification *(this section will describe how to identify the changed material)*

Changeover date code will be notified on later Revision of this PCN.
Changes will be reflected in the following Datasheet Revisions.
AD7124-4 datasheet rev E

Summary of Supporting Information:

Qualification has been performed per Industry Standard Test Methods. See attached Qualification Results.

Supporting Documents

Attachment 1: Type: Other

ADI_PCN_22_0234_Rev_-_RQR10951A.pdf...

Note: If applicable, the device material declaration will be updated due to material change.

ADI Contact Information:

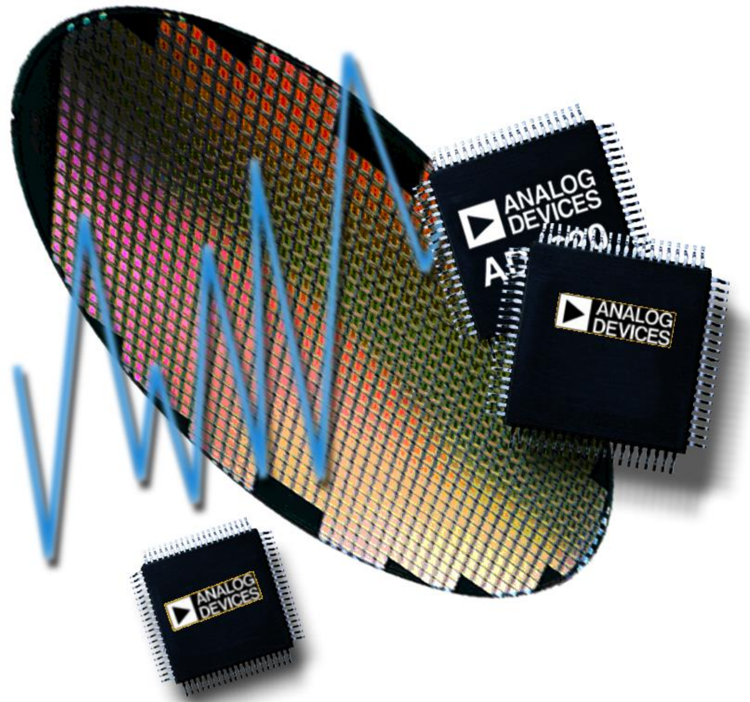
For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.

Americas:	Europe:	Japan:	Rest of Asia:
PCN_Americas@analog.com	PCN_Europe@analog.com	PCN_Japan@analog.com	PCN_ROA@analog.com

Appendix A - Affected ADI Models:

Added Parts On This Revision - Product Family / Model Number (4)

AD7124-4 / AD70/030Z-0RL7	AD7124-4 / AD7124-4BRUZ	AD7124-4 / AD7124-4BRUZ-RL	AD7124-4 / AD7124-4BRUZ-RL7



Reliability Report

Report Title: AD7124-4/-8 TSSOP at ASE (AET) Qualification

Report Number: 20189

Revision: A

Date: 18 December 2022

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the AD7124-4 product in a 24-TSSOP_4.4 package at ASE (AET). The AD7124-4 is a low power, low noise, completely integrated analog front end for high precision measurement applications.

Die/Fab Product Characteristics

Table 1.1: Die/Fab Product Characteristics- 0.18um CMOS

Product Characteristics	Product(s) to be qualified	Product(s) used for Substitution Data		
Generic/Root Part #	AD7124-4	AD7124-4	AD9322	AD81004
Die Id	TMJB25 / C	TMJB25 / B	TMS023 / A	TMFY08/A-T1
Die Size (mm)	2.78 x 3.64	2.78 x 3.64	3.11 x 3.87	8.57 x 3.24
Wafer Fabrication Site	TSMC Fab-11	TSMC Fab-11	TSMC Fab-11	TSMC Fab-11
Wafer Fabrication Process	0.18um CMOS	0.18um CMOS	0.18um CMOS	0.18um CMOS
Die Substrate	Si	Si	Si	Si
Metallization / # Layers	AlCu/5	AlCu/5	AlCu/5	AlCu/5
Polyimide	Yes	Yes	No	No
Passivation	undoped-oxide/SiN	undoped-oxide/SiN	undoped-oxide/SiN	undoped-oxide/SiN

Die/Fab Test Results

Table 2: Die/Fab Test Results - 0.18um CMOS at TSMC Fab-11

Test Name	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS
Early Life Failure Rate (ELFR)	MIL-STD-883, M1015	125°C, 48 Hours	AD81004	Q11314.10	0/120
				Q11314.11	0/40
				Q11314.12	0/120
				Q11314.13	0/120
				Q11314.5	0/120
				Q11314.6	0/120
				Q11314.7	0/120
				Q11314.8	0/120
				Q11314.9	0/120
				Q11314.EL1a	0/200
				Q11314.EL1b	0/200
				Q11314.EL1c	0/200
				Q11314.EL1d	0/200
				Q11314.EL1e	0/200
				Q11314.EL1f	0/40
				Q11314.EL2a	0/200
				Q11314.EL2b	0/200
				Q11314.EL2c	0/200
				Q11314.EL2d	0/200
				Q11314.EL2e	0/200

High Temperature Operating Life (HTOL) [1]	JESD22-A108	125°C<Tj<135°C, Biased, 1,000 Hours	AD7124-4	Q10560.3	0/77
			AD7124-8	Q13197.HO1	0/77
			AD81004	Q11314.1	0/77
				Q11314.17	0/77
				Q11314.HO1	0/77
		135°C<Tj<150°C, 1,000 Hours	AD7124-4	Q10560.16	0/77
				Q10560.17	0/77
		150°C<Tj<175°C, Biased, 500 Hours	AD9322	Q5587.11	0/32
				Q5587.7	0/32
				Q5587.9	0/32
Highly Accelerated Temperature and Humidity Stress Test (HAST) [1]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	AD81004	Q11314.14	0/77
				Q11314.18	0/77
				Q11314.14	0/77
			AD7124-4	Q10560.12	0/77
				Q10560.14	0/77
				Q10560.2	0/77
			AD7124-8	Q13197.HA1	0/77
				Q13197.HA2	0/77
				Q13197.HA3	0/77
				Q18619.1.HA	0/77
				Q18619.2.HA	0/77
				Q18619.3.HA	0/77

[1] These samples were subjected to preconditioning at MSL 3 with 3x reflow peak temp of 260°C prior to the start of the stress test.

Package/Assembly Product Characteristics

Table 3: Package/Assembly Product Characteristics - 24-TSSOP_4.4 at ASE (AET)

Product Characteristics	Product(s) to be qualified	Product(s) used for Substitution Data			
Generic/Root Part #	AD7124-4	AD5203	AD7176-2	AD8802	AD5203
Package	24-TSSOP_4.4	24-TSSOP_4.4	24-TSSOP_4.4	24-TSSOP_4.4	24-TSSOP_4.4
Body Size (mm)	9.70 x 4.40 x 0.86	7.80 x 4.40 x 1.20	7.80 x 4.40 x 1.15	7.80 x 4.40 x 1.15	7.80 x 4.40 x 1.15
Assembly Location	ASE (AET)	ASE (AET)	ASE (AET)	ASE (AET)	ASE (AET)
MSL/Peak Reflow Temperature(°C)	1 / 260°C	1 / 260°C	1 / 260°C	1 / 260°C	1 / 260°C
Mold Compound	Hitachi CEL 9240HF10AK	Hitachi CEL 9240HF10AK	Hitachi CEL 9240HF10AK	Hitachi CEL 9240HF10AK	Hitachi CEL 9240HF10AK
Die Attach	Hitachi EN 4900GC conductive	Hitachi EN 4900GC conductive	Hitachi EN 4900GC conductive	Hitachi EN 4900GC conductive	Hitachi EN 4900GC conductive
Leadframe Material	Copper	Copper	Copper	Copper	Copper
Lead Finish	100Sn	100Sn	100Sn	100Sn	100Sn
Wire Bond Material/Diameter (mils)	2N Gold / 0.80	2N Gold / 0.80	2N Gold / 0.80	2N Gold / 0.80	2N Gold / 0.80

Package/Assembly Test Results

Table 4: Package/Assembly Test Results - TSSOP_4.4 at ASE (AET)

Test Name	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS
Autoclave (AC)[1]	JESD22-A102	121C 100%RH 33.3 psia, 96 Hours	AD7176-2	Q10541.PC4	0/77
				Q10541.PC5	0/77
				Q10541.PC6	0/77
			AD8802	Q10540.PC4	0/77
				Q10540.PC5	0/77
				Q10540.PC6	0/77
			ADG1212	Q10540.PC1	0/77
				Q10540.PC2	0/77
				Q10540.PC3	0/77
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	AD5203	Q10541.HS3	0/77
			AD8802	Q10540.HS2	0/77
			ADG1212	Q10540.HS1	0/77
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	AD5203	Q10541.HA7	0/77
				Q10541.HA8	0/77
				Q10541.HA9	0/77
			AD8802	Q10540.HA4	0/77
				Q10540.HA5	0/77
				Q10540.HA6	0/77
			ADG1212	Q10540.HA1	0/77
				Q10540.HA2	0/77
				Q10540.HA3	0/77

Solder Heat Resistance (SHR)	J-STD-020	MSL-1	AD7124-4	Q20189.1.1	0/30
Temperature Cycling (TC)[1]	JESD22-A104	-65°C/+150°C, 500 Cycles	AD5203	Q10541.TC7	0/90
				Q10541.TC8	0/90
				Q10541.TC9	0/90
			AD8802	Q10540.TC4	0/77
				Q10540.TC5	0/77
				Q10540.TC6	0/77
			ADG1212	Q10540.TC1	0/77
				Q10540.TC2	0/77
				Q10540.TC3	0/77

[1] These samples were subjected to preconditioning at MSL 1 with 3x reflow peak temp of 260°C prior to the start of the stress test.

ESD and Latch-Up Test Results

Table 5: ESD Test Result

ESD Model	Generic/Root Part #	Package	ESD Test Spec	RC Network	Highest Pass Level	Class
FICDM	AD7124-4	24-TSSOP_4.4	JS-002	1Ω, Cpkg	±1000V	C3
HBM	AD7124-8	24-TSSOP_4.4	ESDA/JEDEC JS-001	1.5kΩ, 100pF	±4000V	3A

Table 6: Latch Up Test Result

LU Test Spec	Generic/Root Part #	Passing Current	Passing Over-Voltage	Temperature (T_A)	Class
JESD78	AD7124-4	+200mA, -200mA	+5.4V/+5.4V	25°C	I

Approvals

Reliability Engineer: Allen Lewis Gorrecita

Appendix B - Revision History:

Rev	Publish Date	Effectivity Date	Rev Description
Rev. -	27-Feb-2023	01-Jun-2023	Initial Release